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A Novel Multi-Loop Base Carrier Mark PWM Strategy for Leakage Current Reduction in Grid-Connected Transformerless Inverters

Rajiya Begum Sayyad, Upendar Jalla

Summary — This paper presents a novel multi-loop Base Carrier Mark (BCM) pulse-width modulation strategy to address leakage current challenges in gridconnected transformerless photovoltaic inverters. The proposed approach introduces a combination of sequential level shift, single-loop, two-loop, and three-loop carrier rotation techniques in BCM generation, specifically designed to minimize common-mode voltage variations and suppress leakage current. The method's effectiveness was validated through comprehensive simulation studies using Matlab/Simulink, evaluating eight distinct BCM configurations. Results demonstrate that the proposed multi-loop BCM strategy, particularly in STATE-V configuration, achieves superior leakage current suppression while maintaining high system performance. This configuration reduces leakage current to 2.021 mA, significantly below the VDE 0126-1-1 standard limit of 150 mA (for 40ms fault discontinuity) and the conservative design threshold of 300 mA, without compromising other performance metrics. This configuration reduces leakage current significantly below the standard 300mA limit without compromising other performance metrics. The strategy also demonstrates favorable outcomes in Total Harmonic Distortion (THD < 2% in STATE-II & IV), common mode voltage stability (optimal in STATE-III), and system efficiency (peak performance in STATE-IV). These findings present a significant advancement in transformerless inverter technology, offering a practical solution to the critical challenge of leakage current in grid-connected PV systems. .

Keywords **— Carrier-Based Pulse-width modulation, Transformer-less PV inverter, Total Harmonic**

I. Introduction

The global energy landscape faces significant challenges amid the ongoing pandemic and geopolitical tensions, yet the renewable energy sector, particularly photovoltaics, continues to demonstrate remarkable resilience and growth [1]. This expansion is particularly crucial as the sharp rise in energy prices and geopolitical conflicts, such as the invasion of Ukraine by the Russian Federation, raise serious concerns about energy poverty affecting billions of people. In this context, renewable energy sources, especially photovoltaic and wind technology, must be prioritized to ensure energy security and continuity [2],[3].

Photovoltaic (PV) power systems have emerged as versatile solutions, comprising PV modules and power electronics converters as their fundamental components. These systems can operate in both off-grid and gridconnected configurations, requiring inverters to convert direct current (DC) to alternating current (AC) power [4], [5]. The selection between transformer-based and transformerless inverter topologies presents significant tradeoffs. While transformer-based structures offer galvanic isolation that enhances safety and reliability, they suffer from reduced efficiency and increased system volume, weight, and cost. Conversely, transformerless inverters, despite their advantages, face the critical challenge of leakage current (i_{CM}), which can compromise system safety and reliability [6].

Leakage current poses several significant challenges in transformerless PV systems, including grid current disruption, electromagnetic interference, and corrosion effects on PV panels [7]. Recent research by Yikun Wang (2024) has introduced innovative approaches for minimizing leakage current in three-phase transformerless PV inverters, demonstrating the ongoing efforts to address these challenges [8]. Additionally, studies have proposed advanced suppression methods for single-phase photovoltaic inverters, contributing to the growing body of solutions in this field [9].

In this study, we propose and evaluate multiple PWM techniques based on modified base carrier signals (BCM) for application in a grid-connected single-phase H6-IMPR type transformerless inverter [10]. Our investigation focuses on testing modified sequential level shift, single, two, and three-loop carrier rotation, carrier phase shift, and their derived PWM techniques. The proposed approaches aim to optimize system performance while effectively managing leakage current issues.

The remainder of this paper is organized as follows: Section 2 presents Related Research and Current Developments, section 3 gives a detailed discussion of the H6IMPR transformerless inverter's operating principles, the proposed BCM-based modulation techniques, system design considerations, and leakage current analysis. Section 4 provides comprehensive simulation results validating the effectiveness of the proposed modified BCM-based PWM techniques. Finally, Section 5 concludes the paper with key findings and recommendations for future research directions.

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II. Related Research and Current Developments

A. Topological Innovations

Recent advances in inverter topology design have yielded significant improvements in leakage current management. Tingrui Mao et al. (2024) introduced a novel solution based on active zero-sequence current injections for transformerless grid-connected PV converters, demonstrating enhanced leakage current suppression capabilities [11]. This work builds upon earlier research by Caique et al. (2023), who proposed innovative level modulation switching techniques for leakage current mitigation in transformerless grid-connected PV inverters [3].

B. Modulation Techniques and Control Strategies

The evolution of pulse-width modulation (PWM) techniques has significantly advanced transformerless inverter performance. Christopher Rodríguez-Cortés et al. (2023) provided a comprehensive overview of leakage current reduction methods in single-phase grid-connected inverters, highlighting the importance of advanced modulation strategies [12]. Geye Lu et al. (2023) further contributed to this field by developing an improved leakage-current-based online monitoring method, incorporating asymmetric voltage injection at photovoltaic inverter switching frequencies [13].

Recent developments in PWM techniques have demonstrated promising results in improving system performance. The implementation of improved large midspace vector modulation (ILMSVM) and commonmode subtraction space vector pulse-width modulation (CSSVPWM) has shown effectiveness in suppressing leakage current while enhancing other performance indicators such as total harmonic distortion [14]. Additionally, the Large Small Pulse Width Modulation (LS-PWM) technique has proven successful in reducing stress on both leakage current and switching elements in grid-connected single-phase five-level inverters [15].

C. Performance Enhancement Strategies

Significant progress has been made in developing comprehensive approaches to system optimization. Xiaolong Xiao et al. (2023) proposed innovative strategies for collecting and suppressing leakage current in non-isolated photovoltaic grid-connected systems, demonstrating the potential for improved system reliability [15]. Their work complements earlier research focusing on the development of hybrid/modified modulation techniques which have shown promising results in multilevel inverter applications [3], [12].

The implementation of modified sequential level-shifting PWM techniques in three-phase five-level inverters has demonstrated reduced stress on submodule capacitors [16]. Furthermore, alternative phase-countershifted PWM techniques applied to grid-connected single-phase halfimpedance source-based cascade five-level inverters have shown improved efficiency through various carrier rotation structures [10].

III. Methodology

A. H6-IMPR Inverter Topology and Operating Principles

The improved H6 (H6-IMPR) type transformerless inverter topology forms the foundation of this study [19]. This topology offers enhanced performance characteristics while maintaining fundamental inverter functionality. Fig. 1 illustrates the four basic operating states of the H6IMPR type inverter, showing the power exchange states and zero voltage states in both positive and negative halfcycles.

The inverter's operation can be categorized into four primary modes, each characterized by specific switch states and voltage parameters, as summarized in Table I. During the positive half-cycle (Mode 1), switches S1 and S4 conduct while S2, S3, S5, and S6 remain off, enabling power transfer from the photovoltaic (PV) modules to the grid.

Table I
H6-improved topology switch states S1 - S6.

$S1$	$S2$	$S3$	$S4$	$S5$	$S6$	U_{an}/V	U_{bn}/V	U_{cm}/V	U_{ab}/V	
1	0	0	1	0	0	U_{pv}	0	$U_{\mathrm{pv}}/2$	U_{pv}	P
0	0	0	0	0	1	$U_{\mathrm{pv}}/2$	$U_{\mathrm{pv}}/2$	$U_{\mathrm{pv}}/2$	0	
0	1	1	0	0	0	0	U_{pv}	$U_{\mathrm{pv}}/2$	$-U_{\mathrm{pv}}$	N
0	0	0	0	1	0	$U_{\mathrm{pv}}/2$	$U_{\mathrm{pv}}/2$	$U_{\mathrm{pv}}/2$	0	

In Mode 1, the voltage at point 'a' relative to neutral (U_{an}) equals the PV voltage (U_{PV}), while point 'b' maintains zero potential relative to neutral (U_{bn}). This results in a differential voltage (U_{ab}) of U_{PV} and a common-mode voltage (U_{cm}) of $0.5U_{PV}$.

B. Control Strategy and Modulation Technique

1) Overall Control Architecture: The proposed control strategy employs a cascaded control structure comprising inner current control loops and an outer voltage regulation loop, as illustrated in the enhanced block diagram of Fig. 4. This multi-loop architecture ensures both accurate current injection to the grid and stable DC-link voltage regulation under varying irradiance conditions.

The control system operates in the stationary α-β reference frame to minimize computational complexity while maintaining precise current tracking. A phase-locked loop (PLL) continuously monitors the grid voltage to extract critical synchronization parameters: grid frequency (f_g), angular frequency ($\omega_g = 2\pi f_g$), and phase angle (θ_g). These parameters ensure that the injected current maintains appropriate phase relationship with the grid voltage for desired active and reactive power control.

2) Reference Current Generation: The reference current (i^*_g) for the inner current control loop is synthesized through the following process:

1) The outer voltage controller compares the measured DC-link voltage (V_{pv}) with its reference value (V_{pv}^*) and processes the error through a PI controller:

$$I_{mag} = K_{p,v}(V_{pv}^* - V_{pv}) + K_{i,v}\int (V_{pv}^* - V_{pv})dt \quad (1)$$

where $K_{p,v} = 0.5$ and $K_{i,v} = 20$ are the proportional and integral gains of the voltage controller, tuned to achieve adequate bandwidth (approximately 10 Hz) while maintaining system stability with sufficient phase margin (> 45°).

2) The reference current waveform is constructed by multiplying I_{mag} with the normalized grid voltage template obtained from the PLL:

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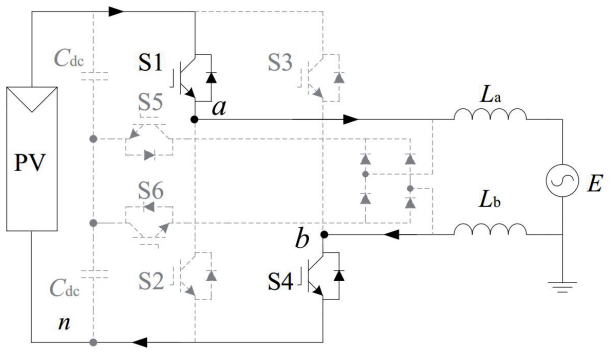
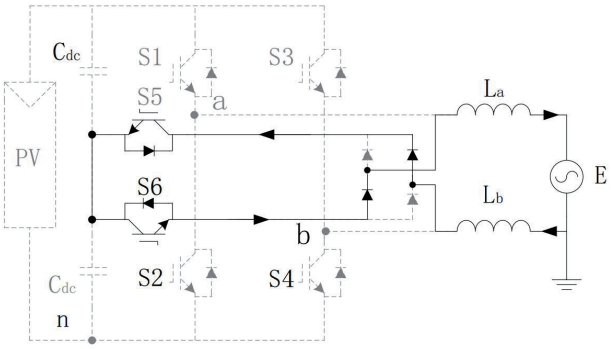
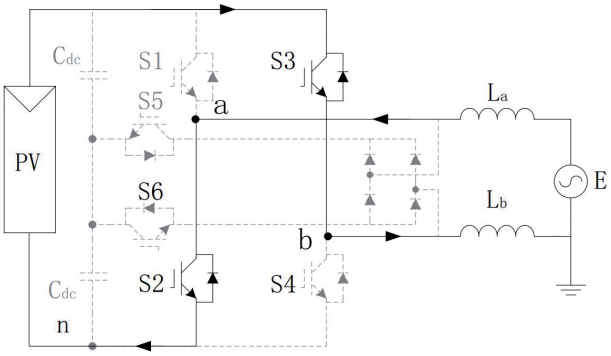


(a) Power exchange state in positive half-cycle

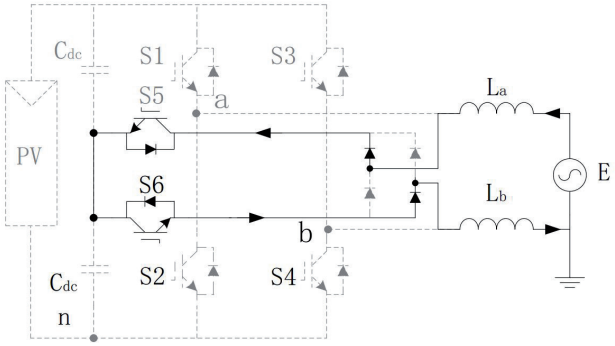


(b) Zero voltage state in positive half-cycle

$$i_g^*(t) = I_{mag} \cdot \sin(\omega_g t + \theta_g) \quad (2)$$



(c) Power exchange state in negative half-cycle



(d) Zero voltage state in negative half-cycle

Fig. 1. Improved H6 type inverter operating cases.

This approach ensures unity power factor operation (inphase current injection) while the magnitude automatically adjusts to balance power flow and maintain DC-link voltage stability.

3) *Inner Current Control Loop:* The inner current control loop regulates the actual grid current (i_g) to track the reference current (i^*_g) with high precision and fast dynamic response. A proportional-resonant (PR) controller is employed due to its superior capability in tracking sinusoidal references with zero steady-state error:

$$G_{PR}(s) = K_p + \frac{K_r s}{s^2 + \omega_0^2} \quad (3)$$

where $K_p = 10$ is the proportional gain, $K_r = 1000$ is the resonant gain, and $\omega_0 = 2\pi f_g = 314.16$ rad/s is the resonant frequency tuned to the grid frequency. The PR controller provides infinite gain at the fundamental frequency (50 Hz), ensuring zero tracking error for sinusoidal references while providing adequate attenuation of harmonic disturbances. The current loop bandwidth is designed to be approximately 1 kHz, providing fast dynamic response while remaining well below the switching frequency to avoid interaction with PWM harmonics.

The current error signal ($e_i = i^*_g - i_g$) is processed through the PR controller to generate the modulation signal ($m(t)$), normalized to the range [-1, 1], which is subsequently compared with the selected BCM carrier waveform to produce switching signals for the H6-IMPR inverter.

4) *BCM Waveform Selection Criteria:* The selection of the eight base carrier mark (BCM) configurations investigated in this study follows a systematic approach based on carrier frequency multiplication, waveform geometry, and their expected impact on common-mode voltage behavior. As illustrated in Fig. 3, the BCM configurations span a wide design space to comprehensively evaluate the relationship between carrier structure and system performance metrics, particularly leakage current suppression.

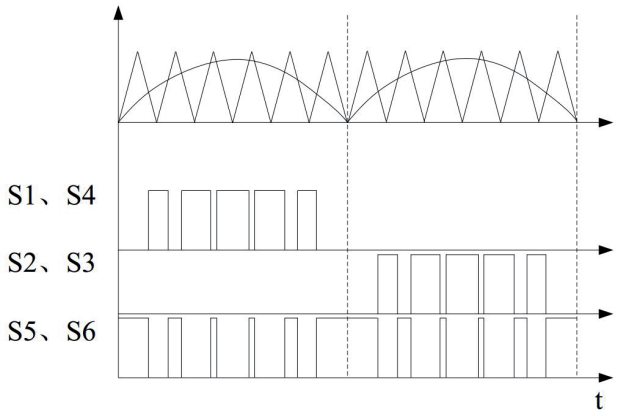


Fig. 2. Basic PWM structure (switching signals)

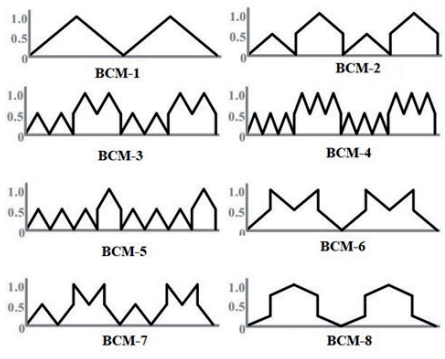


Fig. 3. Principal Base Carrier Mark (BCM) waveforms.

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a) Carrier Waveform Geometry:

The fundamental distinction among BCM configurations lies in their geometric shape, which directly influences switching transition characteristics:

- **Triangular carriers (BCM-1, BCM-6):** Provide linear voltage transitions with constant dV/dt during rising and falling edges. BCM-1 employs two largetriangular waves per fundamental period ($2f_{sw}$), representing the conventional carrier approach. BCM6 uses four medium-sized triangular waves ($4f_{sw}$), offering a balance between switching frequency and harmonic distribution.
- **Trapezoidal carriers (BCM-2, BCM-8):** Incorporate flat-top regions that create extended dwell times at peak carrier values. These plateau regions maintain constant switching states, potentially reducing the number of transitions and associated dV_{cm}/dt spikes. BCM-2 combines trapezoidal and triangular elements, while BCM-8 employs pure trapezoidal waveforms.
- **Multi-triangular carriers (BCM-3, BCM-4, BCM-5, BCM-7):** Feature multiple high-frequency carrier cycles per fundamental period ($6-8f_{sw}$), creating more frequent but smaller-amplitude switching transitions. This category represents the core innovation of the proposed multi-loop approach, where increased carrier frequency enables finer control of common-mode voltage evolution.

b) Carrier Frequency Multiplication:

The effective switching frequency varies significantly across BCM configurations, creating distinct harmonic signatures and switching loss characteristics:

- **Base frequency ($2f_{sw}$):** BCM-1, BCM-2, and BCM8 operate at twice the fundamental switching frequency, providing conventional PWM performance with minimal switching losses but concentrated harmonic content around $2f_{sw}$ and its multiples.
- **Medium frequency ($4f_{sw}$):** BCM-6 doubles the carrier frequency relative to base configurations, offering improved harmonic spreading while maintaining moderate switching losses.
- **High frequency ($6-8f_{sw}$):** BCM-3, BCM-4, BCM5, and BCM-7 employ significantly elevated carrier frequencies, distributing harmonic energy across a broader spectrum. This frequency multiplication enables more uniform common-mode voltage transitions throughout the fundamental period.

c) Loop Rotation Classification:

The multi-loop designation refers to the pattern complexity and phase relationships embedded within carrier structures:

- **Sequential (conventional):** BCM-1, BCM-2, and BCM-8 follow traditional carrier patterns without complex phase rotations.
- **Single-loop rotation:** BCM-3 and BCM-4 implement consistent high-frequency triangular patterns with uniform phase relationships throughout the fundamental period. The small variations between BCM3 and BCM-4 arise from subtle phase adjustments intended to optimize switching instant distribution.
- **Two-loop rotation:** BCM-5 and BCM-6 introduce dual-pattern sequences where carrier characteristics alternate or vary systematically. BCM-5 exhibits non-uniform peak amplitudes, creating asymmetric switching patterns, while BCM-6 maintains uniform amplitudes but at medium frequency.
- **Three-loop rotation:** BCM-7 implements the most complex pattern with three distinct amplitude levels and phase relationships, designed to achieve sophisticated harmonic distribution and common-mode voltage shaping.

d) Common-Mode Voltage and Leakage Current Relationship:

The critical motivation for exploring diverse BCM structures stems from their direct impact on common-mode voltage (V_{cm}) and consequently leakage current. The instantaneous common-mode voltage in the H6-IMPR topology is given by:

$$V_{cm}(t) = \frac{V_{an}(t) + V_{bn}(t)}{2} \tag{4}$$

where V_{an} and V_{bn} are the voltages at inverter output points 'a' and 'b' relative to the neutral point. Different BCM configurations produce distinct switching state sequences, causing variations in $V_{cm}(t)$ evolution. The leakage current through parasitic capacitances (C_{pv}) between PV panels and ground is governed by:

$$i_{cm}(t) = C_{pv}\frac{dV_{cm}(t)}{dt} \tag{5}$$

Therefore, minimizing leakage current requires either: (a) maintaining constant V_{cm} (ideal but often impractical), or (b) minimizing dV_{cm}/dt by controlling switching transition rates and distributions.

Trapezoidal carriers (BCM-2, BCM-8) address this through extended dwell times with zero dV_{cm}/dt during plateau regions. High-frequency multi-triangular carriers (BCM-3 through BCM-7) take an alternative approach by distributing transitions more uniformly in time, potentially reducing peak dV_{cm}/dt values even if the average transition rate increases. The two-loop BCM-5 configuration combines both strategies with varied amplitude peaks and increased frequency, which, as demonstrated in the results, achieves superior leakage current suppression.

e) Design Space Exploration Strategy:

The systematic selection of these eight BCM configurations enables comprehensive evaluation of the multidimensional trade-offs inherent in carrier-based PWM design:

- BCM-1 serves as the baseline conventional triangular carrier reference
- BCM-2 and BCM-8 evaluate the impact of trapezoidal geometry
- BCM-3 and BCM-4 explore single-loop highfrequency approaches
- BCM-5 and BCM-6 investigate two-loop strategies with different frequency-amplitude combinations
- BCM-7 examines the most complex three-loop pattern

This comprehensive exploration strategy ensures identification of optimal configurations for specific performance priorities (leakage current, THD, efficiency, or V_{cm} stability) while revealing fundamental relationships between carrier structure and system behavior. Table II summarizes the key characteristics and design objectives of each BCM configuration.

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TABLE II
CHARACTERISTICS AND DESIGN RATIONALE OF BCM CONFIGURATIONS.

BCM Type	Carrier Structure	Switching Frequency	Pattern Description	Primary Design Objective
BCM-1	Triangular wave	$2\times f_{sw}$	Two symmetric triangular carriers	Baseline conventional triangular carrier PWM
BCM-2	Trapezoidal -triangular	$2\times f_{sw}$	Mixed trapezoidal and triangular	Reduced switching stress with flat-top regions
BCM-3	Multi-triangular (single-loop)	$8\times f_{sw}$	High-frequency small triangular waves	Enhanced harmonic spreading (single-loop)
BCM-4	Multi-triangular (modified)	$8\times f_{sw}$	High-frequency with phase variations	Optimized single-loop with adjusted peaks
BCM-5	Multi-triangular (two-loop)	$6–8\times f_{sw}$	Medium-frequency with varied amplitudes	Balanced V_{cm} control (two-loop rotation)
BCM-6	Triangular (two-loop)	$4\times f_{sw}$	Medium-frequency larger triangular waves	Simplified two-loop with lower switching
BCM-7	Mixed amplitude (three-loop)	$6–8\times f_{sw}$	Non-uniform amplitude triangular pattern	Complex harmonic distribution (three-loop)
BCM-8	Trapezoidal wave	$2\times f_{sw}$	Two symmetric trapezoidal carriers	Minimum switching with extended dwell time

5) PWM Signal Generation Process: The PWM generation process integrates the modulation signal from the current controller with the selected BCM carrier structure: 1) The modulation signal $m(t)$ from the PR controller serves as the reference signal, normalized to the range [1, 1] and synchronized with the grid voltage through the PLL.

2) The selected BCM carrier waveform (BCM-1 through BCM-8) is generated using a dedicated carrier synthesis block that implements the specific geometric pattern and frequency multiplication ratio.

3) Comparator logic generates the primary switching signals by comparing the modulation signal against the BCM carrier. For the H6-IMPR topology with six switches, the switching logic is designed as:

$$S_1, S_4 = \begin{cases} 1, & \text{if } m(t) > 0 \text{ and } m(t) > BCM(t) \\ 0, & \text{otherwise} \end{cases} \quad (6)$$

$$S_2, S_3 = \begin{cases} 1, & \text{if } m(t) < 0 \text{ and } |m(t)| > BCM(t) \\ 0, & \text{otherwise} \end{cases} \quad (7)$$

$$S_5, S_6 = \begin{cases} S_6 = 1, S_5 = 0, & m(t) > 0, m(t) \le BCM(t) \\ S_5 = 1, S_6 = 0, & m(t) < 0, |m(t)| \le BCM(t) \\ 0, & \text{otherwise} \end{cases} \quad (8)$$

(8) This switching logic ensures the proper operating modes detailed in Table I, with switches S5 and S6 providing the freewheeling paths during zero voltage states.

4) Dead-time compensation is implemented to prevent shoot-through conditions during switching transitions. A fixed dead-time of t_{dead} = 2 µs is applied between complementary switch pairs (S1-S2 and S3-S4), with appropriate blanking logic to ensure that both switches in a leg are never simultaneously on.

5) Gate drive signal conditioning includes appropriate voltage levels (0-15V for the SiC MOSFETs specified in Table IV) and current drive capability to ensure fast switching transitions while minimizing switching losses and electromagnetic interference.

6) *Active and Reactive Power Control:* The active and reactive power delivered to the grid can be expressed in the stationary α-β reference frame as:

$$P = \frac{1}{2}(v_{g\alpha} i_{g\alpha} + v_{g\beta} i_{g\beta}) \quad (9)$$

$$Q = \frac{1}{2}(v_{g\beta} i_{g\alpha} - v_{g\alpha} i_{g\beta}) \quad (10)$$

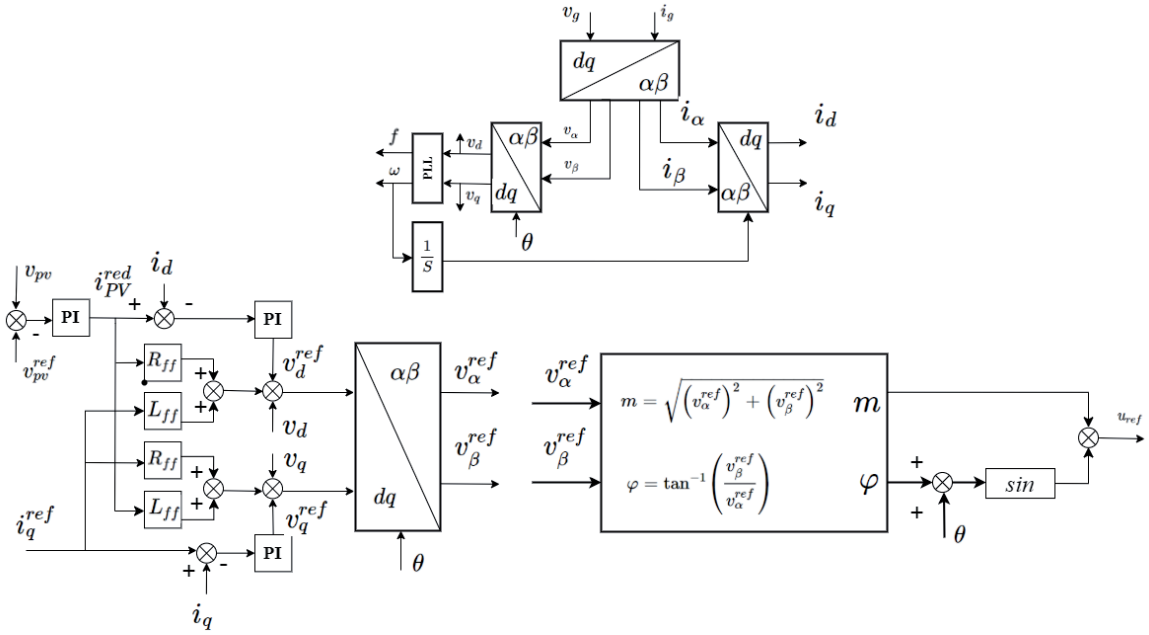

Fig. 4: Block diagram of control strategy for the PWM generation

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For unity power factor operation, the current components in the α-β frame are controlled as:

$$i_{g\alpha} = I_g \cos(\phi) = I_g \tag{11}$$

$$i_{g\beta} = -I_g \sin(\phi) = 0 \tag{12}$$

where $\phi = 0$ represents the phase angle between voltage and current. This control strategy ensures that all delivered power is active power (P) with zero reactive power ($Q = 0$), maximizing system efficiency and minimizing grid current magnitude for a given power transfer. The unity power factor operation also ensures compliance with grid codes and minimizes unnecessary reactive current circulation that would increase losses in both the inverter and grid-side components.

The grid-injected current and voltage waveforms can be expressed in time domain as:

$$v_g(t) = V_g \cos(\omega_g t) \tag{13}$$

$$i_g(t) = I_g \cos(\omega_g t - \phi) = I_g \cos(\omega_g t) \tag{14}$$

where $V_g = 311.13$ V is the peak grid voltage amplitude and $\omega_g = 2\pi f_g = 314.16$ rad/s is the angular frequency corresponding to the 50 Hz grid frequency.

The control block diagram shown in Fig. 4 illustrates the comprehensive control strategy for PWM generation in the grid-connected system.

C. Leakage Current Management

A critical consideration in transformerless inverter design is the management of leakage current, which emerges due to the absence of galvanic isolation between the PV panel and grid system. Fig. 5 illustrates the residual current flow in the PV inverter without transformer.

The parasitic capacitances (C_{PV}) between PV cells/panel and ground lead to charge-discharge cycles with voltage fluctuations, resulting in residual current (i_{cm}) containing both low-frequency and switching high-frequency components. To ensure safe and efficient operation, the leakage current must adhere to standardized limits as specified in Table III.

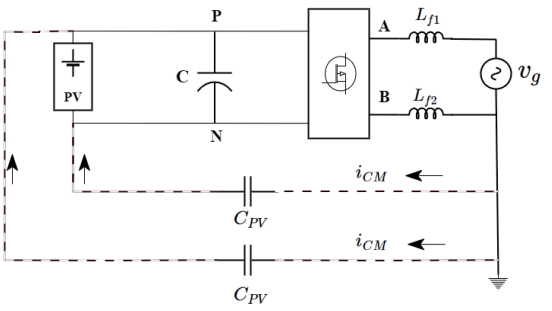

Fig. 5. Residual current flow in PV inverter without transformer.

Table III
Residual Current Limit Values (VDE 0126-1-1)

Fault Discontinuity Time (ms)	Leakage Current (mA)
300	30
150	60
40	150

These regulatory limits vary based on fault discontinuity time, with maximum allowable currents ranging from 30 mA to 150 mA depending on the duration of the fault condition. This regulatory compliance is essential for maintaining system safety and electromagnetic compatibility while minimizing power losses.

IV. Simulation Study

The simulation study was implemented using **Matlab/Simulink R2021b** environment with a fixed-step solver and a time step of 1×10^{-7} seconds to ensure accurate representation of high-frequency switching dynamics. The control algorithms were implemented using standard Simulink blocks.

Fig. 6 presents the comprehensive block diagram of the simulated system, illustrating the interconnection between the PV source, H6-IMPR inverter topology, LCL filter network, grid connection, and control subsystems. The control structure encompasses both inner current control loops and outer voltage regulation, with the PLL providing grid synchronization. The BCM generator block produces various carrier waveforms (BCM-1 through BCM-8) which are compared with the sinusoidal reference to generate appropriate gate signals for switches S1-S6.

The simulation investigation was conducted to evaluate the performance characteristics of a grid-connected transformerless H6-IMPR inverter system. The fundamental configuration, illustrated in Fig. 6, comprises an inverter coupled to the mains through a filtering network. The key parameters monitored during the simulation include the grid-injected current (I_g), the post-filter mains connection point voltage (V_g), and the inverter input bus voltage (V_{pv}). The system generates appropriate switching signals for the inverter's switches (S_1-S_6) based on various Base Carrier Mark (BCM) configurations.

The simulation environment was implemented using Matlab/Simulink, with the system parameters detailed in Table IV.

Table IV
System simulation parameters.

Parameter	Value
DC bus voltage V_{da}	400V
Output voltage V_g	311. 13 V
Grid frequency f_g Nominal	50 Hz
Power	14kW
Switching Frequency f_{sw}	10kHz
Filter Inductance (L_{f2},L_{f1})	6mH
Filter Capacitor C_f	2.0nF
Parasitic Capacitor C_{pv}	18nF
Switches (SCT3080ALGC11)	V_{dss} = 650V,$R_{ds,ON)}$ = 80mΩ,V_{sd} = 3.2V
Diodes (APT15D60B)	V_r = 600V,V_F = 1.9V

To comprehensively evaluate the system's performance, eight distinct states were examined, each corresponding to a different Base Carrier Mark configuration (BCM-1 through BCM-8), as outlined in Table V.

Table V
States simulation study.

State	Base Carrier Mark (BCM)
I	BCM-1
II	BCM-2
III	BCM-3
IV	BCM-4
V	BCM-5
VI	BCM-6
VII	BCM-7
VIII	BCM-8

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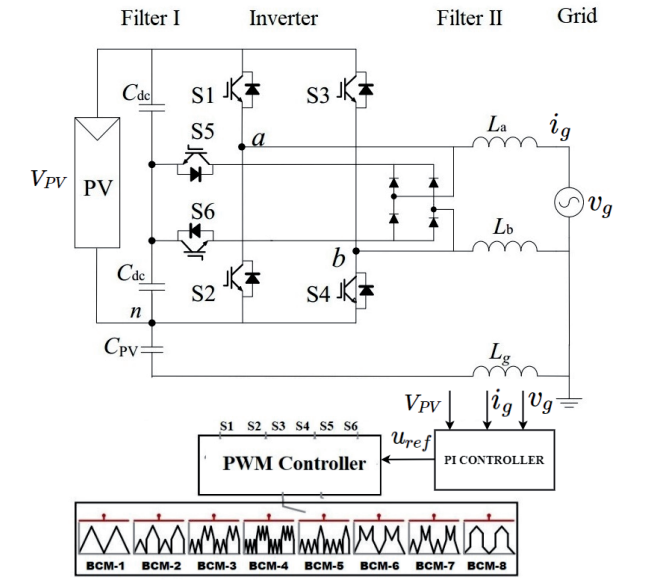
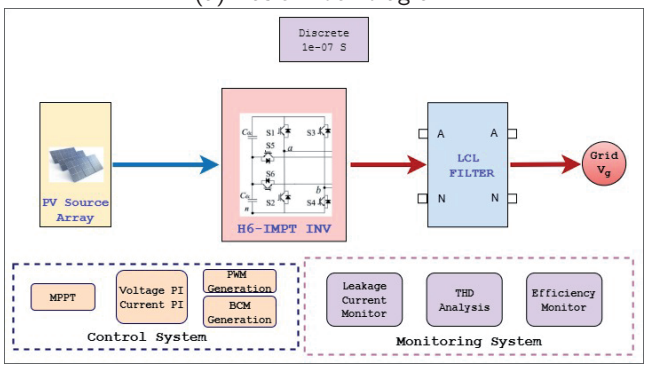
The analysis focused on several key performance metrics: inverter efficiency (η), Total Harmonic Distortion (THD) of the output current, common mode voltage (V_{cm}), and leakage current (i_{cm}).



(a) Basic Block diagram



(b) MATLAB simulation block diagram

Fig. 6: Basic block diagram of the simulated system showing inverter connection to grid through filter

A. Total Harmonic Distortion Analysis

The analysis of Total Harmonic Distortion (THD) in the grid-injected current revealed significant variations across different BCM configurations, as illustrated in Fig. 7. The measured THD values ranged from 0.04% to 2.95%, demonstrating the substantial impact of carrier structure selection on output current quality.

STATE-II and STATE-IV PWM control schemes demonstrated the most favorable THD performance with exceptionally low values of 0.04%, representing nearideal sinusoidal current injection. STATE-I (0.09%) and STATE-VI (0.11%) also exhibited excellent performance. Conversely, STATE-V exhibited the highest THD at 2.95%, followed by STATE-VIII (2.07%) and STATEVII (2.02%). Despite these variations, all configurations remained well below the IEEE 519-2014 standard limit of 5% THD, ensuring full compliance with international power quality requirements.

An important observation is the inverse relationship between leakage current suppression and THD performance. STATE-V, which achieves the lowest leakage current (2.021 mA), exhibits the highest THD (2.95%). This trade-off suggests that asymmetric carrier patterns optimizing common-mode voltage behavior for leakage current reduction simultaneously introduce harmonic distortion. Conversely, STATE-II and STATE-IV achieve optimal THD but with moderate leakage current levels. The selection between these configurations depends on application priorities: BCM-2 or BCM-4 for maximum power quality, or BCM-5 for maximum leakage current suppression while maintaining regulatory compliance.

State	THD (grid current)
I	0.09%
II	0.04%
III	1.13%
IV	0.04%
V	2.95%
VI	0.11%
VII	2.02%
VIII	2.07%

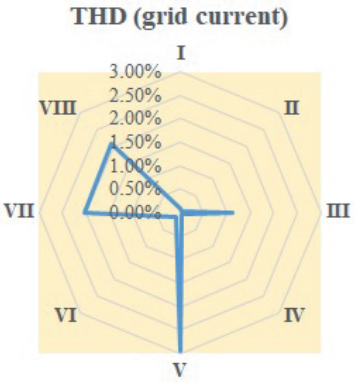


Fig. 7. THD grid current results for different type BCM

B. Common Mode Voltage Analysis

The common mode voltage (V_{cm}) analysis, presented in Fig. 8, revealed interesting patterns across different control configurations. Theoretically, the V_{cm} value should equate to $V_{pv}/2$. The experimental results demonstrated that STATE-III PWM control achieved the closest approximation to this ideal value compared to other configurations. This finding suggests that STATE-III PWM control offers superior common mode voltage characteristics, potentially contributing to enhanced system stability and reduced electromagnetic interference.

State	V_CM (AVERAGE)
I	201.315
II	201.312
III	201.134
IV	201.155
V	201.412
VI	201.221
VII	201.356
VIII	201.251

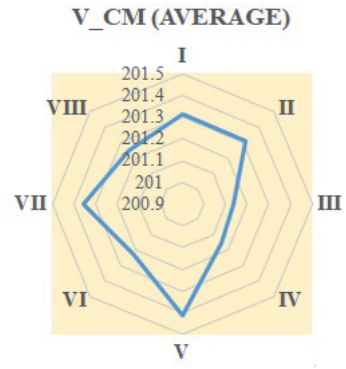


Fig. 8: Average common mode voltage V_{cm} results

C. Leakage Current Analysis

The investigation of leakage current (I_{cm}), depicted in Fig. 9, demonstrated that all PWM control configurations maintained leakage current levels below the standardspecified limit of 300mA. STATE-V PWM control exhibited the most favorable performance with the lowest leakage current values, while STATE-VIII PWM control resulted in the highest leakage current measurements. This variation in leakage current characteristics highlights the importance of control strategy selection in managing system safety and compliance requirements.

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TABLE VI
MEASURED PEAK LEAKAGE CURRENT VALUES FOR ALL BCM CONFIGURATIONS.

State	BCM Type	Peak I_{cm} (mA)	Compliance Status
I	BCM-1	5.441	√Pass
II	BCM-2	4.2641	√Pass
III	BCM-3	3.5451	√Pass
IV	BCM-4	3.3541	√Pass
V	BCM-5	2.021	√Pass (Best)
VI	BCM-6	5.4491	√Pass
VII	BCM-7	4.5999	√Pass
VIII	BCM-8	7.7551	√Pass
VDE 0126-1-1 Limit (40ms discontinuity)			150 mA
Conservative Design Limit			300 mA

It should be noted that while Table III presents the regulatory limits specified in VDE 0126-1-1 standard, industrial practice often adopts more conservative design thresholds. Throughout this work, we reference a conservative design limit of 300 mA to ensure robust safety margins across varying environmental and operating conditions, while maintaining compliance with the stricter 150 mA regulatory limit for 40ms fault discontinuity time.

The investigation of leakage current (I_{cm}), depicted in Fig. 9 and quantified in Table VI, demonstrated that all PWM control configurations maintained leakage current levels significantly below both the VDE 0126-1-1 standard limit of 150 mA (for 40ms fault discontinuity time) and the conservative design threshold of 300 mA. The measured peak leakage current values ranged from 2.021 mA (STATE-V) to 7.7551 mA (STATE-VIII), representing merely 1.35% to 5.17% of the regulatory limit.

STATE-V PWM control exhibited the most favorable performance with 2.021 mA, demonstrating a 73.9% reduction compared to STATE-VIII. Other notable lowleakage configurations include STATE-IV (3.3541 mA) and STATE-III (3.5451 mA). Even the worst-performing configuration maintains leakage current at only 2.59% of the conservative design threshold, demonstrating the effectiveness of all proposed multi-loop BCM strategies. The superior performance of STATE-V is attributed to its two-loop carrier rotation pattern, which effectively minimizes common-mode voltage variations and reduces high-frequency components in the parasitic capacitance charging/discharging cycles.

D. EFFICIENCY ANALYSIS

The efficiency analysis, illustrated in Fig. 10, revealed a clear correlation between BCM configuration and system performance. Under the tested operating conditions, STATE-VIII PWM control, utilizing the BCM VIII waveform, demonstrated the lowest efficiency levels. Conversely, STATE-IV PWM control, implementing the BCM-IV waveform, achieved the highest efficiency ratings. This significant variation in efficiency metrics emphasizes the critical role of BCM waveform selection in optimizing system performance.

State	I_CM (RMS)
I	5.441
II	4.2641
III	3.5451
IV	3.3541
V	2.021
VI	5.4491
VII	4.5999
VIII	7.7551

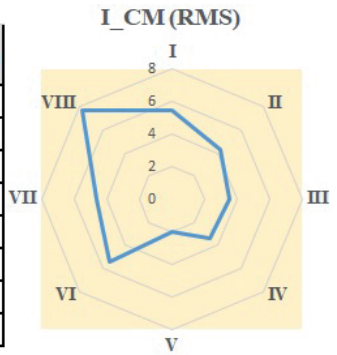

Fig. 9 Leakage Current values for different type BCM control

State	η (efficiency)
I	98.103
II	98.101
III	98.1
IV	98.141
V	98.079
VI	98.103
VII	98.051
VIII	97.781

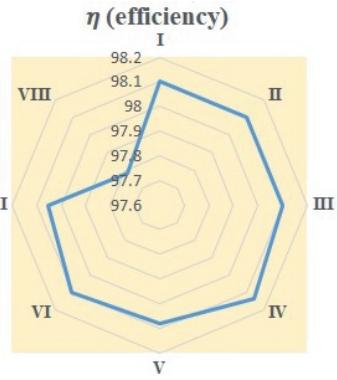

Fig. 10. Efficiency values for different BCM control

The comprehensive analysis of these performance metrics provides valuable insights into the optimization of grid-connected transformerless inverter systems. The results demonstrate that different BCM configurations offer distinct advantages and trade-offs across various performance parameters, necessitating careful consideration in system design and implementation.

V. CONCLUSION

This research introduces and validates a novel multiloop BCM-based PWM strategy for leakage current reduction in transformerless inverters. The comprehensive evaluation of eight distinct BCM configurations reveals the superior performance of the proposed approach, particularly in addressing the critical challenge of leakage current suppression. The STATE-V configuration of the multi-loop BCM strategy demonstrates exceptional capability in minimizing leakage current while maintaining compliance with safety standards, representing a significant advancement in transformerless inverter technology. The study's findings highlight the effectiveness of combining different carrier rotation techniques in BCM generation, resulting in optimized system performance across multiple metrics. While STATE-V excels in leakage current suppression, other configurations show strengths in specific areas: STATEII & IV achieves superior THD performance, STATEIII optimizes common mode voltage characteristics, and STATE-IV maximizes system efficiency. This comprehensive performance evaluation provides valuable insights for system designers, enabling informed decisions based on specific application requirements. The proposed multi-loop BCM strategy represents a practical and effective solution to one of the most significant challenges in transformerless PV inverter design. Future research could focus on developing adaptive switching strategies between different BCM configurations based on real-time grid conditions and exploring the integration of artificial intelligence techniques for optimal BCM selection. These advancements would further enhance the applicability of transformerless inverters in next-generation renewable energy systems.

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