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A Resistive Voltage Divider for Power Measurements

SUMMARY

The paper presents a resistive voltage divider (RVD), developed for power measurements at much higher frequencies than the traditional 50 Hz. The design of the RVD and the methods of its evaluation are described. The RVD is intended to be used in a digital sampling wattmeter application based on National Instruments PXI-4461 Dynamic Signal Analyzer. The design of the divider includes individual copper guards for each resistor, driven by the auxiliary chain of resistors. To reduce the leakage currents, the PTFE terminals are applied between pins of the resistors and the printed circuit board.

KEYWORDS

resistive voltage dividers; power measurement; PXI-4461; guarding

INTRODUCTION

The resistive voltage divider (RVD) presented in this paper was designed with the main goal to be used in a digital sampling wattmeter application based on National Instruments PXI-4461 Dynamic Signal Analyzer. Since the peak input voltage of PXI 4461 Dynamic Signal Analyzer cards is constrained to 42.4 V maximum, the mains voltage (i.e. 230 V) has to be lowered using an instrument transformer or a voltage divider. In [1] a voltage instrument transformer (VIT), developed for the same application was presented. The development of the RVD was triggered with a goal to further decrease the ratio and phase angle error of the voltage transducer, thus improving the accuracy of the wattmeter.

As high-precision voltage transducers in power measurements, two types of transducers are eligible for the implementation: inductive voltage dividers (IVD) [2], and recently, resistive voltage dividers (RVD) [3-5]. The need for the much wider frequency range than traditional 50 Hz, required the use of RVDs instead of IVD. The goal was to extend the frequency bandwidth from 50 Hz to at least 3 kHz. In the audio frequency range the performance of IVDs are not satisfying, or their design is very difficult. Consequently, the frequency range of IVDs is too narrow, and the nonlinearity of their ferromagnetic core induces the harmonic distortion of the voltage [2-5]. The main purpose of this paper is to present the design of the RVD recently developed within our research group at FER-ZOEEM, with the special emphasis on the design issues as the guarding, leakage currents and the measurement procedures for the determination of the accuracy. The nominal ratio of the resistive divider is V_{in}/V_{out}=560 V/ 10 V.

The paper is organized as follows: in Section II the design principles of the RVD are described, Section III presents the measurement system based on NI 4461 cards for the characterization of the RVD. Section IV gives the measurement results of the implementation of the proposed method using a NI PXI system and Section V gives the uncertainty analysis. Finally, Section VI are conclusions.

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DESIGN PRINCIPLES

Fig. 1 presents the equivalent circuit diagram of the guarded resistive divider. The parasitic capacitances are marked in dashed lines, C_0 is the input capacitance of the instrument measuring the output voltage (including cable capacitance). R_{gn} are resistances of the auxiliary chain of resistors.

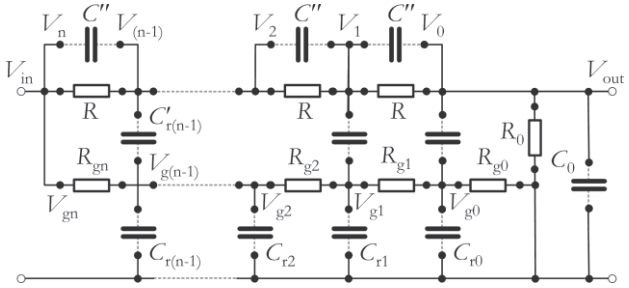

Fig. 1. Equivalent circuit diagram of the divider

The ratio of the divider is defined as:

$$V_{in} / V_{out} = nR / R_0 + 1 \quad (1)$$

The leakage current through the main printed circuit board (PCB) could increase the phase and ratio errors of RTD. In order to reduce this effect, the resistors consisting the divider are soldered on the polytetrafluoroethylene (PTFE) insulated terminals, as depicted in the Fig. 2, similarly to the design described in [6].

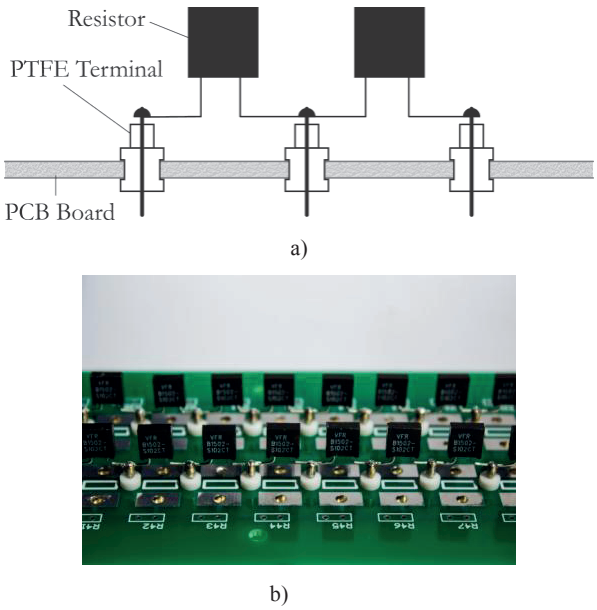

Fig. 2. Lateral view of resistor mounts: a) connection diagram b) photo of the device

The divider is consisted of n=25 resistors with the nominal value equal to R=4.4 kΩ and one resistors with the nominal value R_0=2 kΩ, which gives according to (1) the nominal ratio of the divider 560 V/10 V. All resistors are Vishay S series bulk metal foil (BMF), high precision resistors, model number S102C, with the ambient power rating 0.6 W at 70C. The typical temperature coefficient of resistance (TCR), declared by Vishay is ppm/C, for all resistors in the divider. The balanced TCRs in all resistors of the divider minimize the change of the ratio of the divider for different input voltages, and enables measuring of the ratio and phase angle responses of the divider at the voltage lower than nominal.

Fig. 3 presents the complete circuit diagram of the divider with the auxiliary chain of resistors and guards. Resistors R_1 – R_{26} are resistors consisting the divider, with the values R_1 – R_{25}=R and R_{26}=R_0. Resistors R_{27} – R_{53} are forming the auxiliary chain. The resistors in the auxiliary chain are chosen in such a way that the guard of the each resistor in the divider is approximately at the potential equal to the potential of the half of the corresponding resistor in the main chain. In such a way the voltages at the parasitic capacitances from Fig. 1 are minimal, and consequently the influence of the parasitic capacitances are reduced. Taking into account the standard values of the resistors, the resistors in the auxiliary bridge are taken with the nominal values R_{27}= 2.2 kΩ, R_{28} – R_{51}=4.7 kΩ, R_{52}=R_{53}=2.2 kΩ. The resistors R_{28} – R_{51} in the auxiliary chain are standard metalfilm resistors, chosen from a lot of 88 resistors. The resistances of all resistors in the set were measured prior the assembling using the 4-wire technique and a 61/2 digit multimeter Keysight 34465A, and 24 resistors with mutually closest values were chosen for the assembling. To reduce the loop area and the parasitic inductance, and in the same time to ensure the more compact physical dimensions of the divider, the resistors in the divider in the final layout of the PCB are arranged in two parallel rows (Fig. 4), connected together with a short piece of the coaxial cable Amphenol 223/U with the sleeve cable at the corresponding resistor guard potential. Fig. 4 depicts the PCB with the resistors and guards during the assembling.

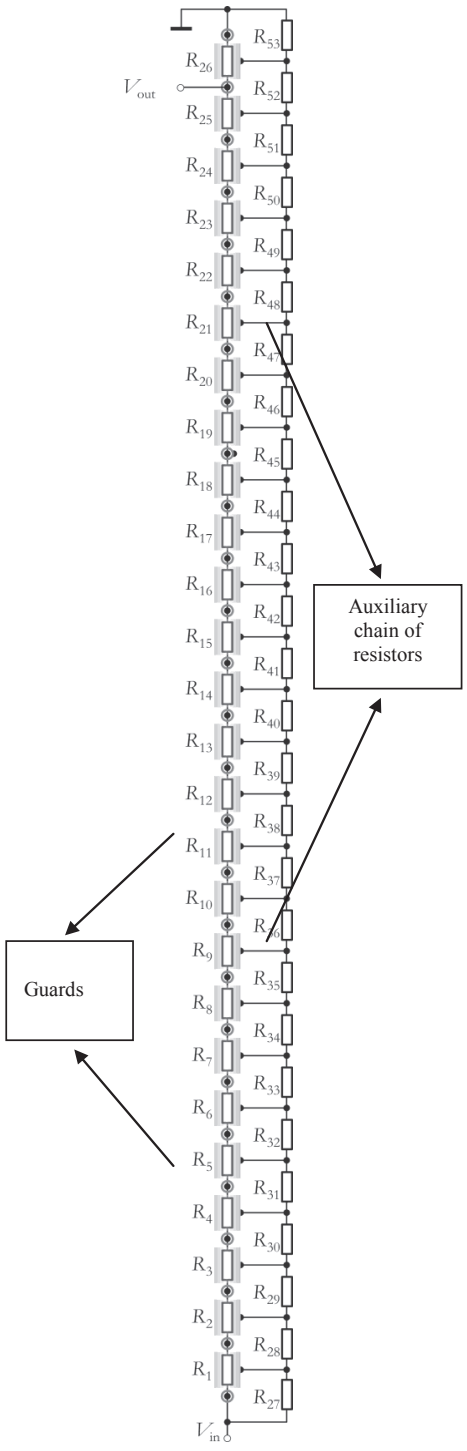

Fig. 3. Circuit diagram of the divider with the auxiliary chain of resistors and guards

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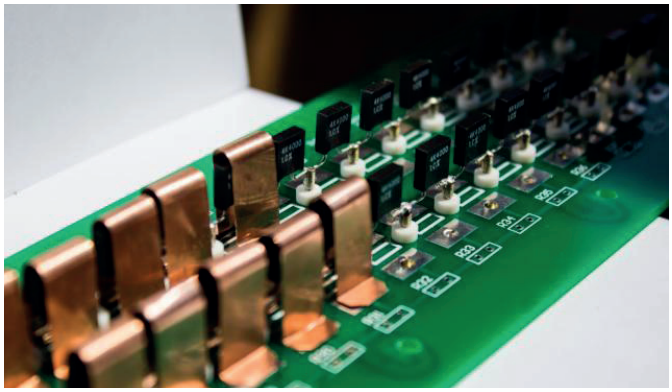

Fig. 4. The divider during assembling

MEASUREMENT SYSTEM

The measurement set-up was consisted of National Instruments PXI system, equipped with the acquisition cards (DAQ) NI PXI 4461. Time clock synchronization was accomplished using the internal PCI bus that divides 33 MHz clock. The additional synchronization of the start of the measurement process was achieved using a PXI trigger bus. Fig. 5 presents the block diagram of the measurement system, while the Fig. 6 shows the measurement set-up. The coaxial cable for the connection of the RVD to the NI 4461 card was the same that will be used in the sampling wattmeter application. In such a way, the load impedance, which affects transfer function of the divider, is the same as in the wattmeter application. The load impedance is consisted of the cable capacitance shunted by the input impedance of the card (1 MΩ paralleled by 217 pF). All inputs of the cards were configured in differential configuration.

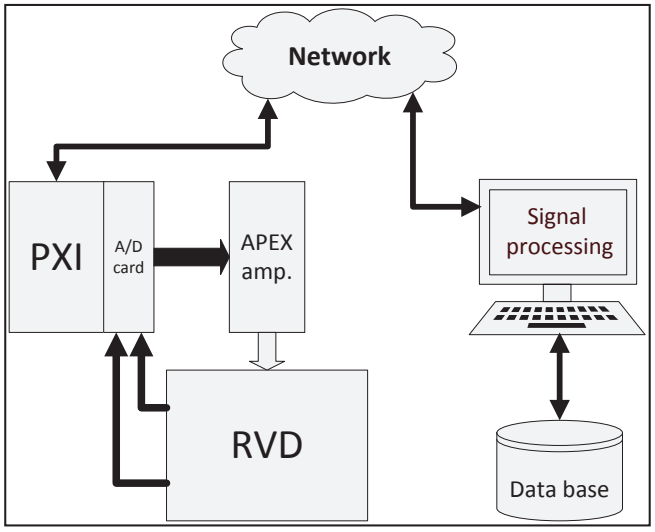

Fig. 5. Block diagram of the measurement system

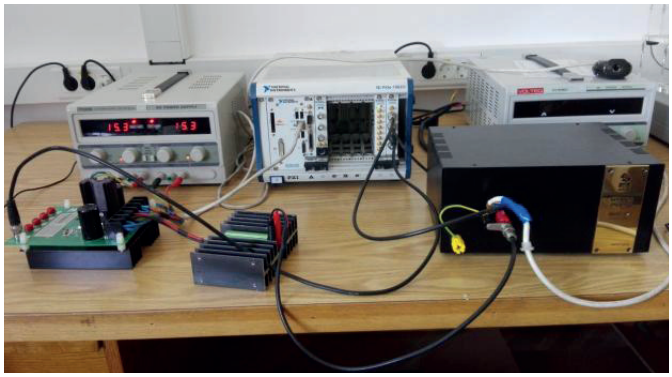

Fig. 6. Measurement set-up

The PXI system generates the stimulus signal, which is fed to the power amplifier based on Apex MP111 power operational amplifier and EK57 evaluation kit. The signal from the power amplifier is brought to the input of the divider. The input and output voltages of the RVD are brought to a NI PXI 4461 card.

The needed software was entirely programmed in-house in the NI LabView environment. The measurement process starts with the definition of the frequency range, magnitude and the set of replicate measurement for the averaging process. The communication between LabView application and the PXI system is accomplished using the Ethernet protocol and the institutional local area network (LAN), thus enabling distant start and control of the measurements. All the parameters are transferred to the PXI client that adjusts the magnitude and frequency, performs the measurements and sends the measurement results to the personal computer.

MEASUREMENT RESULTS

The measurement results are consisted of two main parts: the measurement of the ratio of the divider, and the measurement of the phase shift of the RVD.

The ratio and the phase shift are measured in a wider frequency bandwidth than defined by the international standard EN 50160, which defines measurement of the harmonics and interharmonics up to the 40th harmonic of the fundamental frequency. The frequency response of the ratio and phase shift have been measured in two ranges:

(i) Lower range, covering two sets of first 50 harmonics of fundamental harmonics equal to 50 Hz and 60 Hz (frequencies up to 3 kHz)

(ii) Extended range, covering the frequencies up to 50 kHz

$$k = \frac{V_{in}}{V_{out}}$$

The ratio of the divider is in all subsequent results defined as , where V_{in} denotes the input voltage and V_{out} denotes the output voltage. The phase angle is defined as $\varphi = \alpha_{out} - \alpha_{in}$ where $\alpha_{out} -$ denotes the phase angle of the output signal and α_{in} denotes the phase angle of the input signal. Fig. 7 presents the ratio of the divider for the frequencies below 3 kHz. Fig. 8 presents the phase shift for the same frequency range. Fig. 9 and 10 present the ratio and the phase angle of the divider for the extended frequency range.

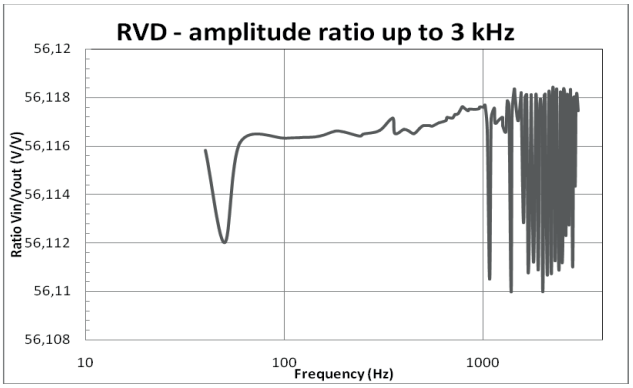

Fig. 7. Ratio of the RVD for the freqeuncies bellow 3 kHz

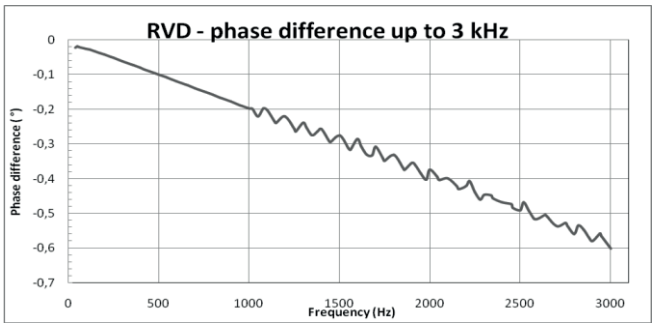

Fig. 8. Phase angle of the RVD for the freqeuncies bellow 3 kHz

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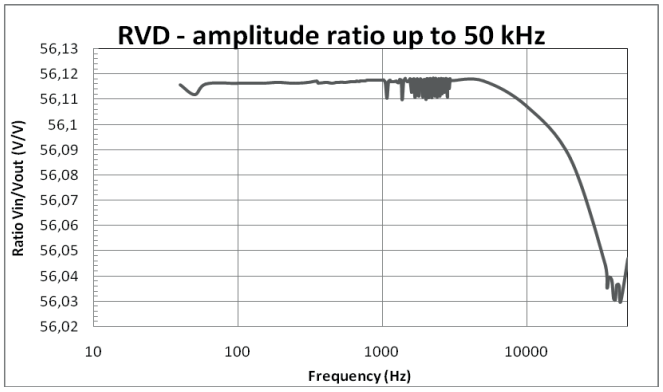

Fig. 9. Ratio of the RVD for the extended frequency range

Frequency (Hz)

Fig. 9. Ratio of the RVD for the extended frequency range

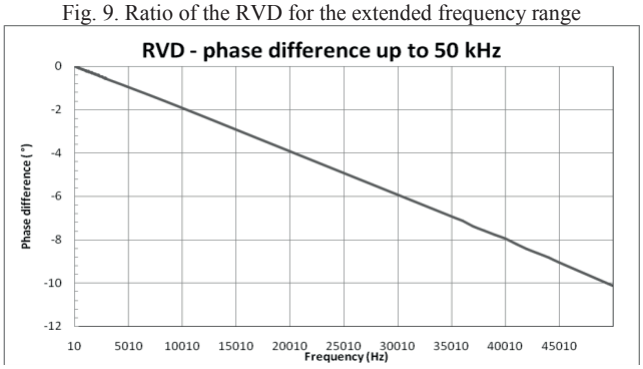

Fig. 10. Phase angle of the RVD for the extended frequency range

UNCERTAINTY ANALYSIS

The digitizer NI-PXI4461 has a two-channel 24-b sigma-delta A/D converter. A very significant parameter in characterizing a digitizer is the integral nonlinearity (INL), and its INL is smaller than 1 μV/V at frequencies higher than 40 Hz. The large INL (maximum INL is more than 80 μV/V) appears at lower frequencies, accompanied with a significant hysteresis, which can be atributed to thermal effects [7]. For 1 V signal amplitude, 1 V input range and 51.2 kS/s sampling frequency and simultaneous sampling, the digitizer's full metrological properties are as follows [8]: the temperature coefficients of the magnitude and phase are 7.4 μV/V/K and 0.000008 /K. The standard deviation of the magnitude of the voltage ratio is 2.3 μV/V. The deviation of the magnitude of the voltage ratio from the nominal value is within 3 μV/V. The phase deviation is less than 16 μ.

At 40 Hz the ratio of the RVD is 56.116 V/V where the nominal ratio is 56 V/V. The ratio of the RVD at 100 Hz is 56.116 V/V, and at 3 kHz it equals 56.117 V/V. According to Fig. 7, for the frequency range below 3 kHz it reaches the maximum value equal to 56.118 V/V and minimum value equal to 56.110 V/V, both for the frequencies between 1kHz and 3 kHz. Therefore, the maximum ratio error for the first 60 harmonics is below 0.011 %.

The phase angle at 40 Hz is -0.0211, and at 100 Hz it is -0.0250. Finally, the phase angle is -0.6010at 3 kHz. From the Fig. 6 it may be concluded that the phase angle changes linearly with the slope -0.2/kHz.

CONCLUSION

The resistive voltage divider, intended for the use in a sampling wattmeter application is developed and manufactured.

According to these results, the errors of the divider are within satisfying limits, and it yields significantly better results than a previously developed instrument voltage transformer [1] for a laboratory sampling wattmeter based on the NI 4461 DAQ. The RVD will be used in line with a set of precise current shunts of the cage type already developed at our laboratory.

The presented design is also a good basis for the further improvements that will possibly decrease the phase angle error. It can be achieved using the active elements (e.g. operational amplifiers) and compensation of the load capacitance, which is the main factor affecting the phase angle error. Those improvements will be necessary if the improved design of the RVD will be implemented in a future power standard.

REFERENCES

[1] M. Dadić, K. Petrović, R. Malarić, "FEM analysis and design of a voltage instrument transformer for digital sampling wattmeter," MIPRO 2017 Proceedings, Opatija, 2017, pp. 174-178.

[2] B.P. Kibble, G.H. Rayner, Coaxial AC Bridges, Adam Hilger, Bristol, 1984.

[3] T. Hagen and I. Budovsky, "Development of a Precision Resistive Voltage Divider for Frequencies up to 100 kHz," 2010 Conference on Precision Electromagnetic Measurements Digest (CPEM), June 13-18, 2010, Daejeon, Korea, pp. 195-196.

[4] K. E. Rydler, S. Svensson, and V. Tarasso, "Voltage Dividers with Low Phase Angle Errors for a Wideband Power Measuring System," 2012 Conference on Precision Electromagnetic Measurements Digest (CPEM), June 16-21, 2012, Ottawa, Ontario, Canada, pp. 382-383.

[5] E. Mohns, W.G. Kuerten Ihlenfeld, "A Precise Active Voltage Divider for Power Measurements," 2004 Conference on Precision Electromagnetic Measurements Digest (CPEM), June 27 – 02 July, 2004, London, UK, pp. 84-85.

[6] W. Lei, Zhu Zongwen, H. Hongtao, L. Min, L. Lijuan, L. Zuliang, "Resistive Voltage Divider with Two Stage Voltage Buffer for Harmonic Measurement," 2012 Conference on Precision Electromagnetic Measurements Digest (CPEM), 01–06 July, 2012, Washington DC, USA, pp. 148-149.

[7] F. Overney, A. Ruefenacht, J.P. Braun, B. Jeanneret and P.S Wright, "Characterization of Metrological Grade Analog-to-Digital Converters Using a Programmable Josephson Voltage Standard," IEEE Trans. Instrum. Meas., vol. 60, no. 7, pp. 2172-2177, July 2011.

[8] R. Rybski, J. Kaczmarek, M. Koziol, "A High-Resolution PXI Digitizer for a Low-Value_Resistor Calibration System, " IEEE

[9] Trans. Instrum. Meas., vol. 62, no. 6, pp. 1783-1788, June 2013.

[10] M. Dadić, P. Mostarac, R. Malarić, "Wiener Filtering for Real-Time DSP Compensation of Current Transformers over a Wide Frequency Range," IEEE Transactions on Instrumentation and Measurement, vol. 66, no. 11, pp. 3023-3031, November 2017.